UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO. : 7,278,715 B2
APPLICATION NO. : 10/827045
DATED : October 9, 2007
INVENTOR(S) : Trudy L. Benjamin et al.

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In column 9, line 40, after "~A1," delete "A2 ... A7" and insert -- ~A2 ... ~A7 --, therefor.

In column 9, line 66, delete "PRE2 PRE6" and insert -- PRE2 ... PRE6 --, therefor.

In column 31, line 12, delete "EVAL1" and insert -- EVAL2 --, therefor.

In column 36, line 39, delete "~A2, ~A7" and insert -- ~A2, ... ~A7 --, therefor.

In column 40, line 39, after "Timing" insert -- pulse 958 turns on third evaluation transistor 556. A control pulse 960 in control signal CSYNC 824 turns on control transistor 558 and forward direction signal DIRF 842 discharges to a low voltage level at 962.

The next series of six timing pulses shifts the high voltage level shift register output signal SO12 to the next shift register cell 403k that provides a high voltage level shift register output signal SO11. Shifting continues with each series of six timing pulses until each shift register output signal SO1-SO13 has been high once. After shift register output signal SO1 is high, the series of high voltage level shift register output signals SO 830 stops. The shift register 402 can be initiated again by providing a control pulse, such as control pulse 870, coincident with a timing pulse from timing signal T2 804.

In reverse direction operation, a control pulse from CSYNC 824 is provided coincident with a timing pulse from timing signal T6 at 820 to set the direction of shifting to the reverse direction. Also, a control pulse from CSYNC 824 is provided coincident with a timing pulse from timing signal T2 804 to start or initiate the shift register 402 shifting a high voltage level signal through the shift register output signals SO1-SO13.

FIG. 13 is a block diagram illustrating one embodiment of two address generators 1000 and 1002 and six fire groups 1004a-1004f. Each of the address generators 1000 and 1002 is similar to address generator 400 of FIG. 9 and fire groups 1004a-1004f are similar to fire groups 202a-202f illustrated in FIG. 7. The address generator 1000 is electrically coupled --.

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In column 41, line 1, after "1004a-" delete "1 004c" and insert -- 1004c --, therefor.

In column 41, line 13, after "1008a-" delete "1 008f" and insert -- 1008f --, therefor.

In column 41, line 14, after "SEL1," delete "SEL2, SEL6" and insert -- SEL2, ... SEL6 --, therefor.

In column 41, line 15, after "1004a-" delete "1 004f and insert -- 1004f --, therefor.

In column 42, line 26, delete "SELL" and insert -- SEL1 --, therefor.

In column 46, line 14, delete "SELL" and insert -- SEL1 --, therefor.

In column 57, line 50, in Claim 4, delete "round" and insert -- around --, therefor.

In column 60, line 12, in Claim 30, delete "claims" and insert -- claim --, therefor.

Signed and Sealed this

Seventh Day of July, 2009

John Doll

JOHN DOLL
Acting Director of the United States Patent and Trademark Office